REMARKS

A replacement drawing sheet has been submitted. A replacement abstract has been submitted. Claims 1, 10, and 16 have been amended. Claims 2-9, 11-15, and 17-22 have been canceled. New claims 23-29 have been added. Claims 1, 10, 16, and 23-29 remain pending in the application. Reexamination and reconsideration is respectfully requested.

No new matter has been added. Support for the amendments and new claims may be found in figure 1, and the discussion of figure 1 in the specification.

A replacement sheet for drawing sheet 1 has been submitted. The page number has been amended, and the labels NODE_A and NODE_B have been reversed. Drawing sheet 1 as originally filed is incorrectly numbered (it should be numbered 1/2 instead of 1/1). In addition, in Figure 2 as originally filed, NODE_A and NODE_B are reversed relative to the description in the specification (for example, paragraph [0016]). The description in the specification is correct.

In the Office Action dated 07/18/2008, the examiner objected to the Abstract and provided suggested changes. The Abstract has been amended to incorporate the examiner's suggestions, and additional changes have been made to reflect claim amendments.

In the Office Action dated 07/18/2008, claim 15 was objected to for lack of antecedent basis. Claim 15 has been canceled.

Claims 1-5, 9-11, 13-15, and 20-22 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Number 6,201,418 (Allmon). The following discussion will be limited to claims 1, 10, and 16 as amended.

For purposes of illustration, assume that in the present application, figure 1, input signal IN_H is high and input signal IN_L is low, as illustrated in figure 2. When CLK is low, both NODE_A and NODE_B are precharged high, as illustrated in figure 2. Note in particular that NODE_A may be actively driven high by any of three different paths in transistor group 29. That is, in addition to precharge transistor 16, NODE_A may also be driven high by NODE_B through transistor 23 when NODE_B is low, and NODE_A

may also be driven high by transistors 32 and 33 when input signal IN_L is low and C_L (NODE_A inverted) is low. Therefore, when CLK transitions from low to high, precharge transistor 16 turns off, but NODE_A is still being actively driven high by transistors 32 and 33. In addition, later when NODE_B goes low, NODE_A is also driven high by transistor 23. As a result, NODE_A is actively driven high continuously by at least one of three different paths from the time CLK goes low (precharge phase), during the transition of CLK from low to high, and on through the evaluation phase, until some future time when IN_H is low at the time CLK goes high.

Claim 1 has been amended to specify: "actively maintaining a second node continuously in its predetermined state from a time before the clock signal changes from the first level to the second level, until a time after the first node changes from its predetermined value." Claim 10 has been amended to specify: "wherein the circuit element actively maintains the second node at its predetermined state continuously from a time before the first node starts changing from its predetermined state until a time after the first node changes from its predetermined state." Claim 16 has been amended to specify: "while a second node within the plurality is actively maintained in an initial state, continuously from a time before the timing signal causes the first node to start changing to its finalized state until a time after the first node changes to its finalized state."

In the circuit in Allmon, there is a period of time immediately after the clock transition during which the node that remains at the precharge level is not actively being driven high. In Allmon, figure 1, for the node that is to remain high, none of the pull-up transistors is actively pulling that node high in the period between when CLK goes high and one of the PREOUT signals goes low. During that brief time interval, the node that is supposed to remain high is susceptible to soft errors.

From the above discussion, one of the three paths for holding a node high is controlled by one of the input signals combined with the state of the node. New claim 23, dependent on claim 1, specifies: "wherein the second node is actively maintained in its predetermined state by one of the plurality of signals and the state of the second node." New claim 29 specifies: " driving a second node in the plurality of nodes to the precharge

state by a second input signal and by a signal corresponding to the state of the second node.

Claims 10, 11, and 13-15 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Number 4,910,713 (Madden). The following discussion will be limited to claim 10 as amended.

The discussion above regarding Allmon applies equally to Madden. In Madden, figure 1, for the output signal that is supposed to remain high, none of the pull-up transistors is pulling that output signal high in the period between when AMP STROBE goes high and the other output signals goes low. During that brief time interval, the output line that is supposed to remain high is susceptible to soft errors.

Claims 6-8 and 12 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Allmon in view of U.S. Patent Number 5,504,703 (Bansal). Claims 6-8 and 12 have been canceled.

In the present application, figure 1, for the node that transitions from the precharge state to a low state, there is a "keeper" transistor (18 or 19) that holds the node low after a time delay. For example, when transistors 14 and 21 drive NODE_B low, then after a delay by inverter 4, transistor 19 also holds NODE_B low. From paragraph [0020], the keeper transistor for the node that is supposed to remain high (transistor 18) is susceptible to causing soft errors, and delaying the signal to transistor 18 further reduces susceptibility to soft errors by making sure that transistor 18 is not being driven during the initial part of the evaluation phase. New claims 24 and 26 specify delaying a signal that causes circuitry to actively maintain a node at its second state.
In the present application, paragraph [0021], pull-up transistors (for example, 30, 31, 32, and 33) may be made larger than pull-down transistors to further reduce susceptibility to soft errors. New claim 27, dependent on claims 26 and 10, further specifies that at least one transistor in the circuit element that maintains the second note at its predetermined state is larger than any transistor in the circuit element that can actively maintain the second node in a second state.

In view of the above, it is believed all of the pending claims are now in condition for allowance.

Respectfully submitted,

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